G	R	B	G	R	B	G	R
B	G	R	B	G	R	B	G
R	B	G	R	B	G	R	B
G	R	B	G	R	B	G	R

FIGURE 1B

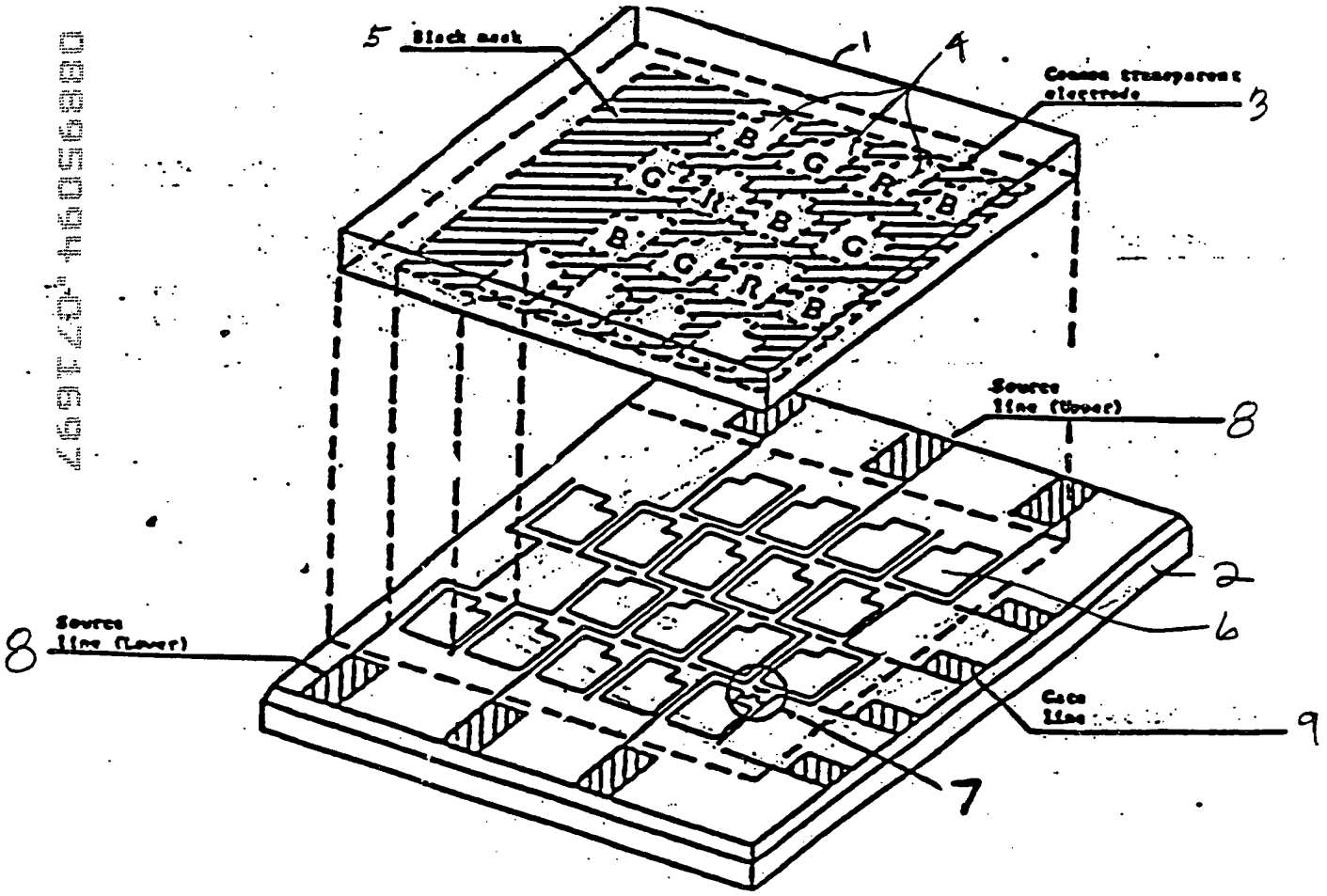


FIGURE 1A

Fig. 2 Camera Block Diagram

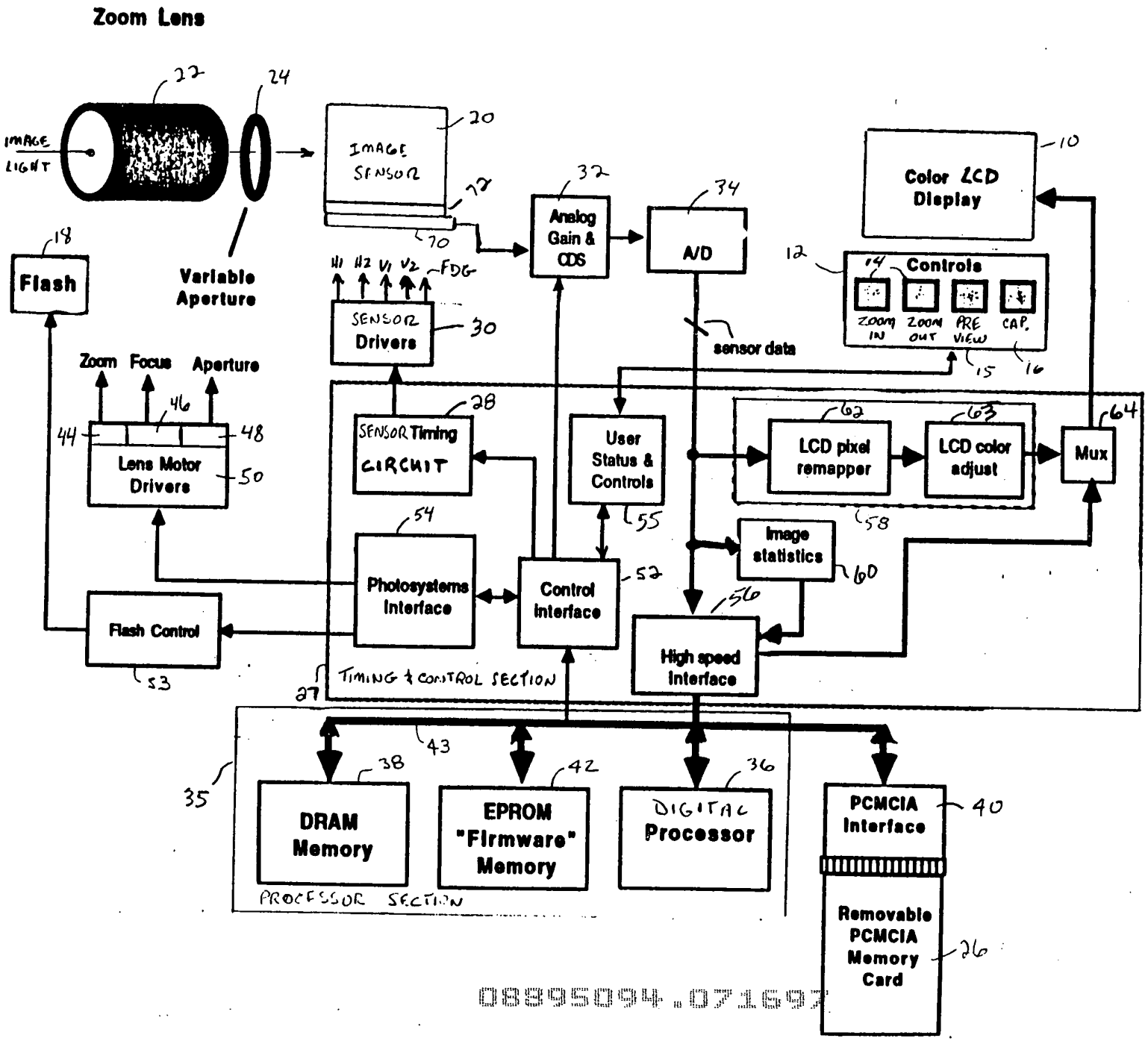


Fig. 3 A

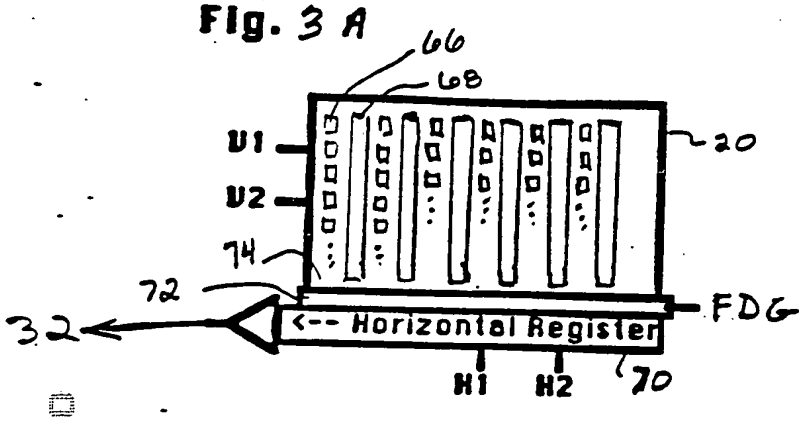


Fig. 3 B

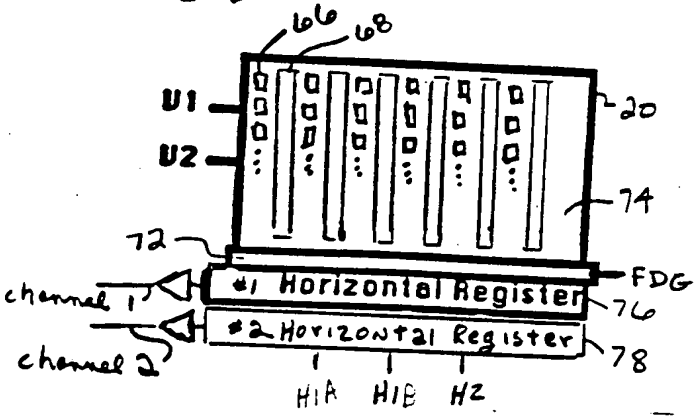


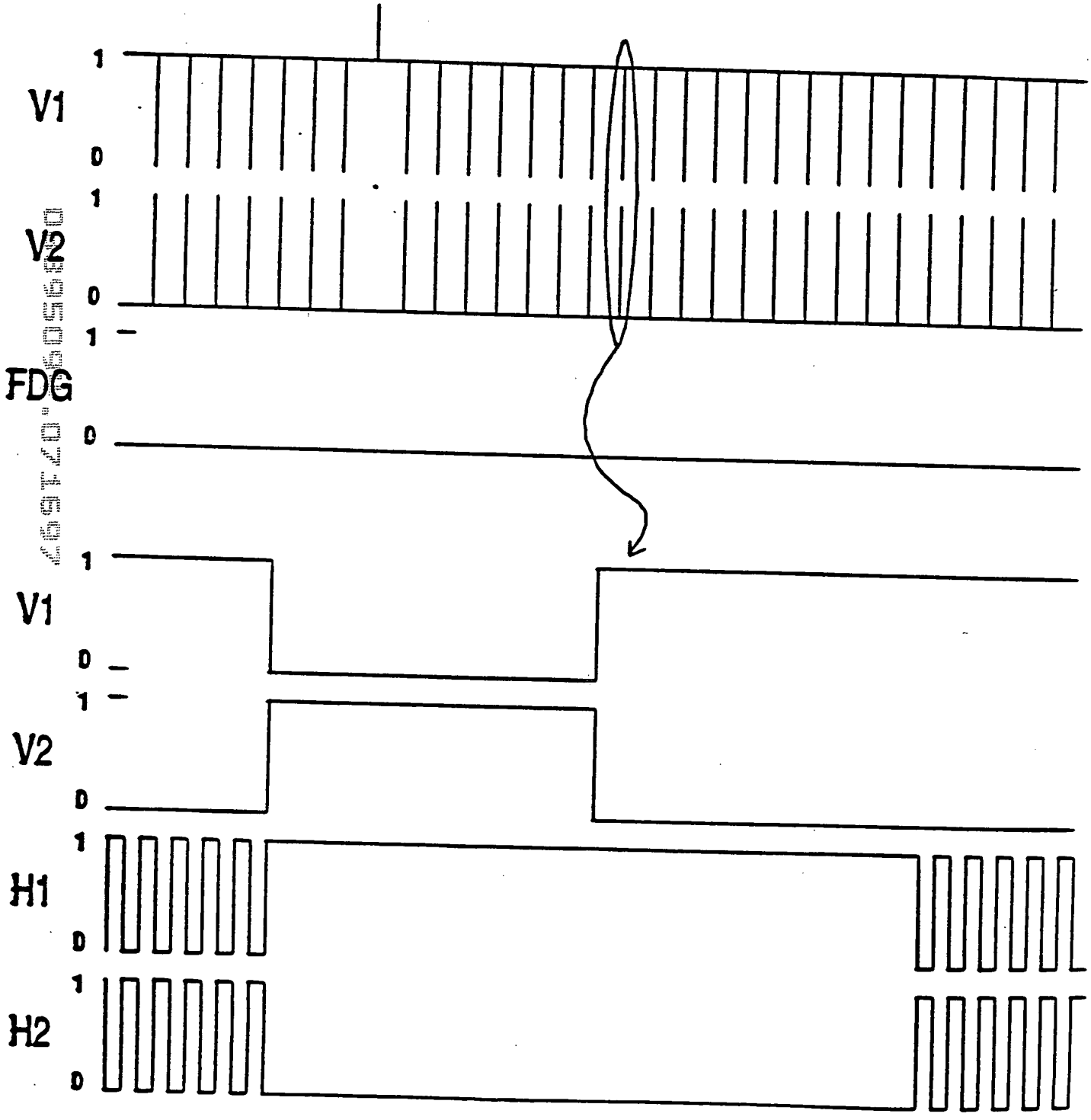
Fig. 4

CCD lines

line 1	G	R	G	R	G	R	G	R
line 2	B	G	B	G	B	G	B	G
line 3	G	R	G	R	G	R	G	R
line 4	B	G	B	G	B	G	B	G
line 5	G	R	G	R	G	R	G	R
line 6	B	G	B	G	B	G	B	G
line 7	G	R	G	R	G	R	G	R
line 8	B	G	B	G	B	G	B	G

FIG 5

Still mode timing diagram



Pseudo-Interlace mode timing diagram

FIG 6a

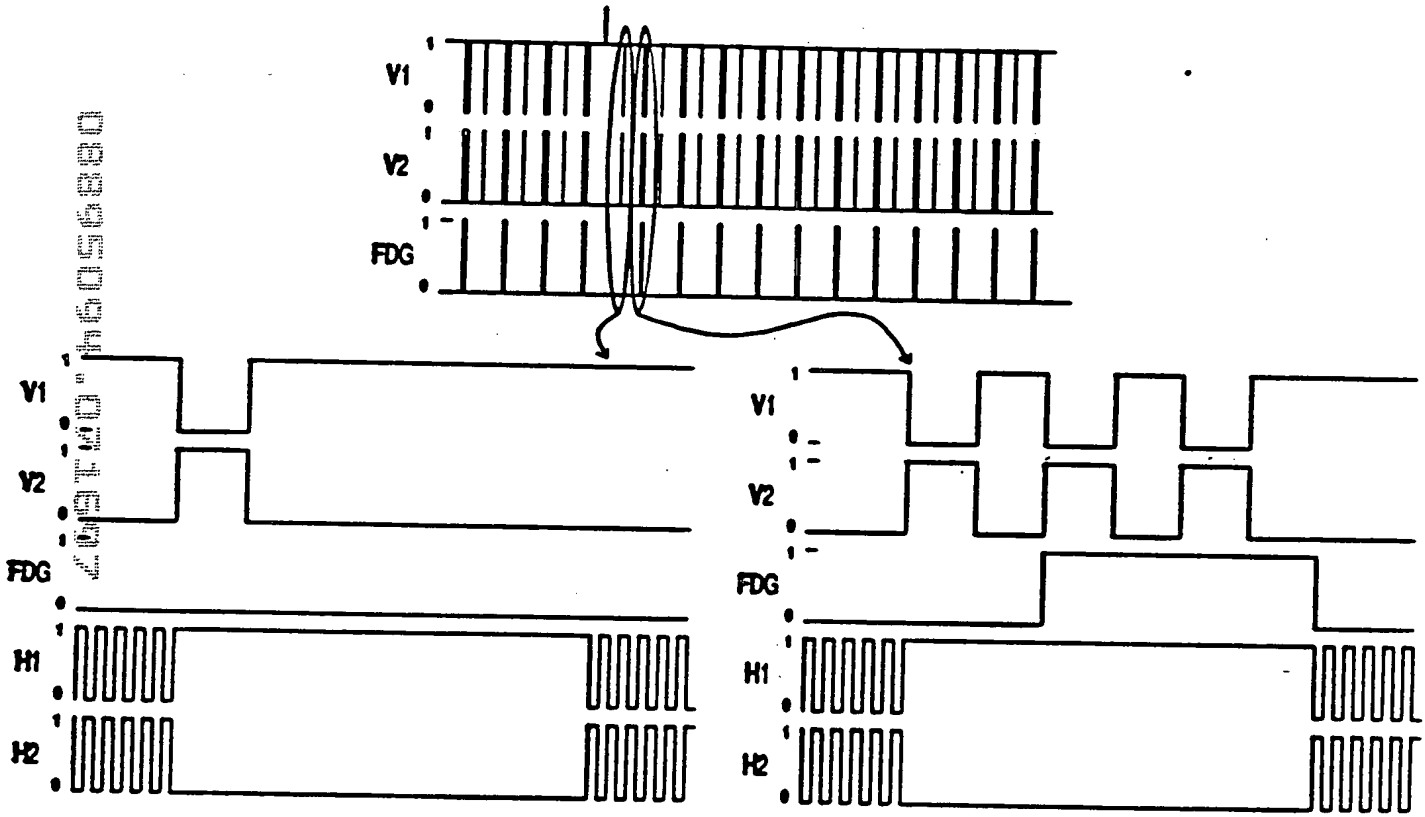


FIG 6b

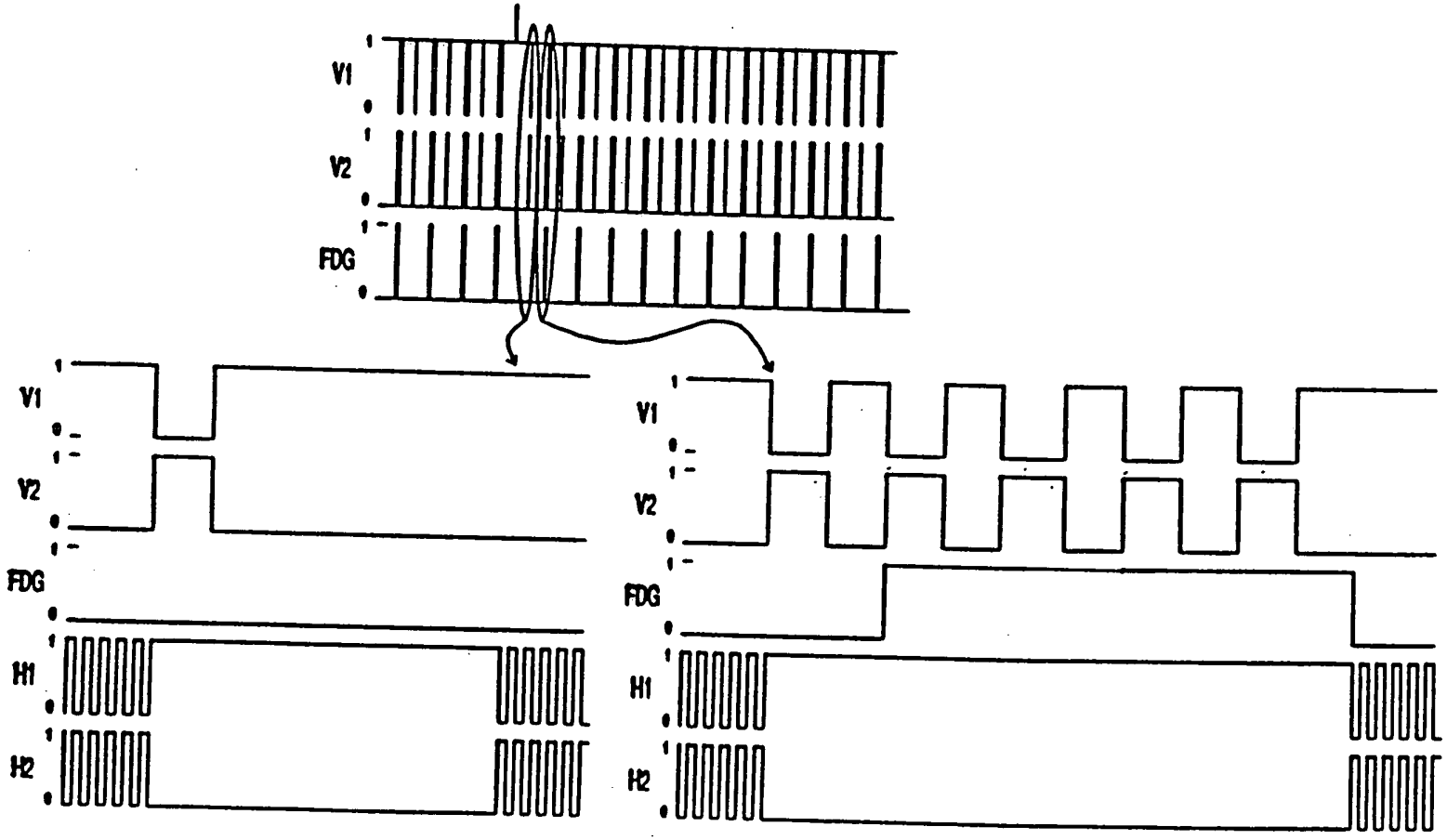


Fig. 7

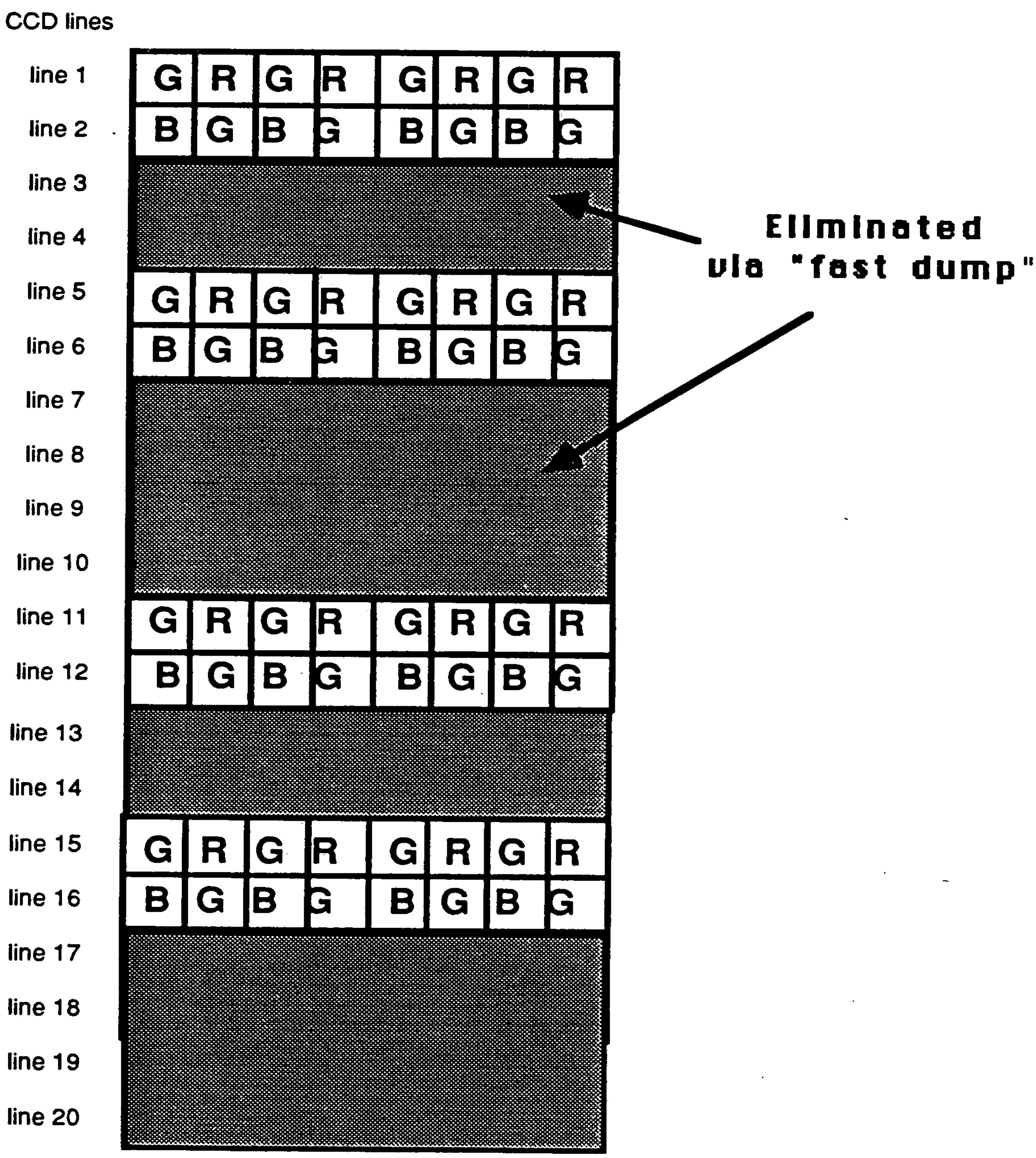

CCD lines
line 1
line 2
line 3
line 4
line 5
line 6
line 7
line 8
line 9
line 10
line 11
line 12
line 13
line 14
line 15
line 16
line 17
line 18
line 19
line 20
G R G R G R G R
B G B G B G B G
Eliminated via "fast dump"

Fig. 8 Preview Mode LCD Processing

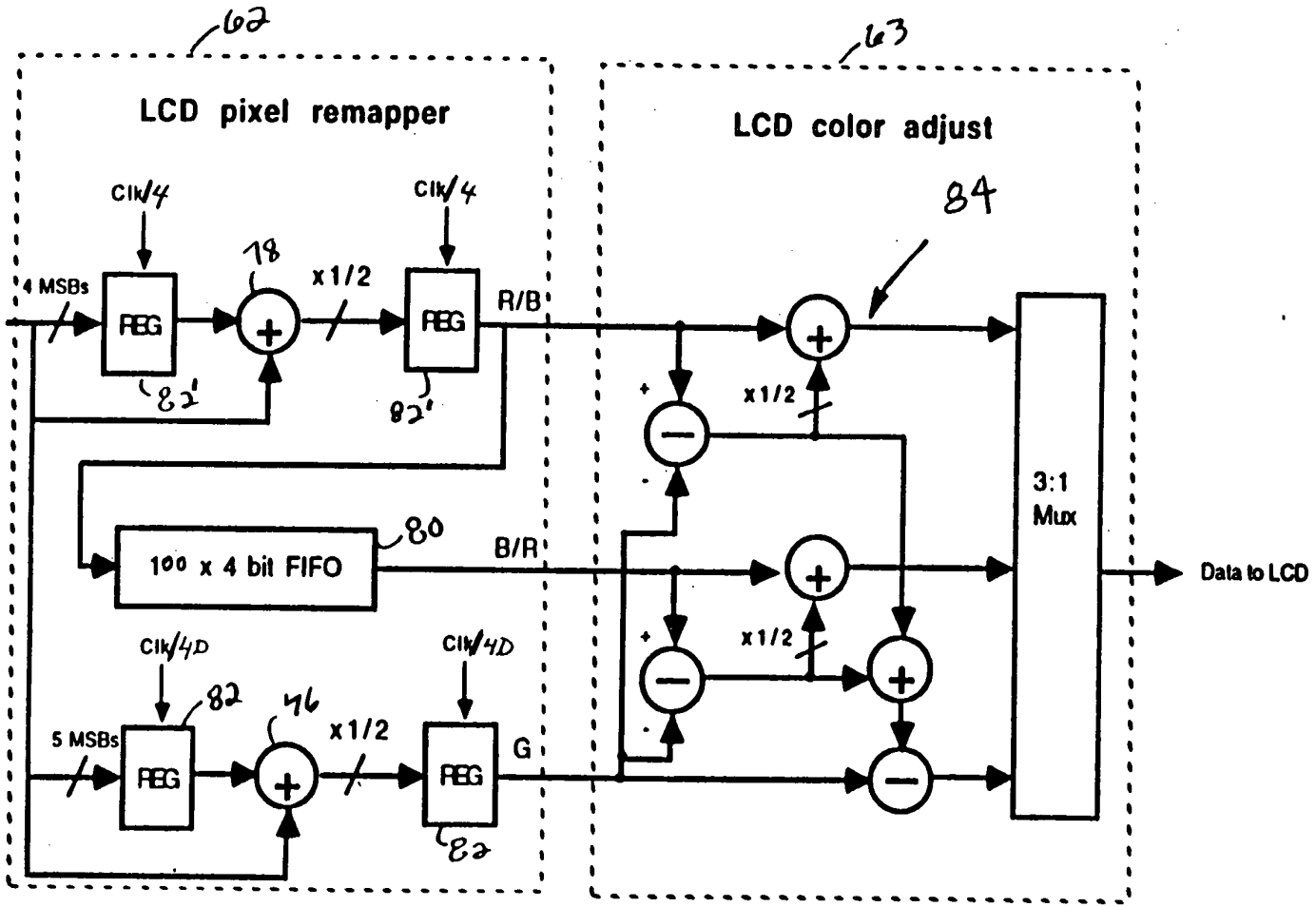


Image exposure / white balance statistics

Calculate average signal level in 4 x 6 matrix of blocks for each of R,G, and B.

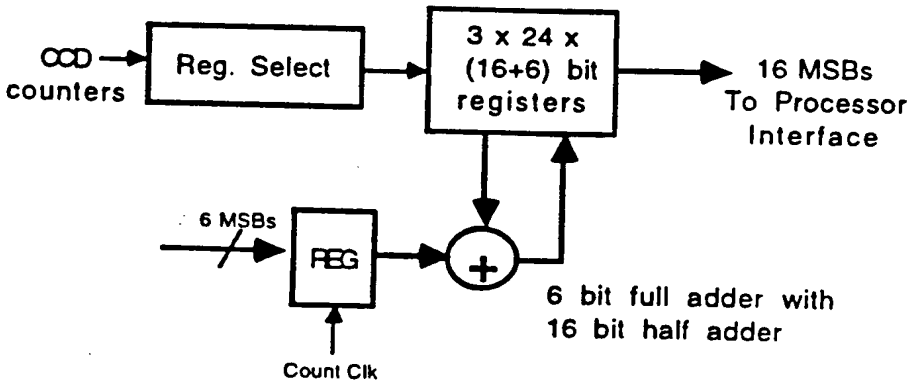


FIG. 9A

Image focus statistics

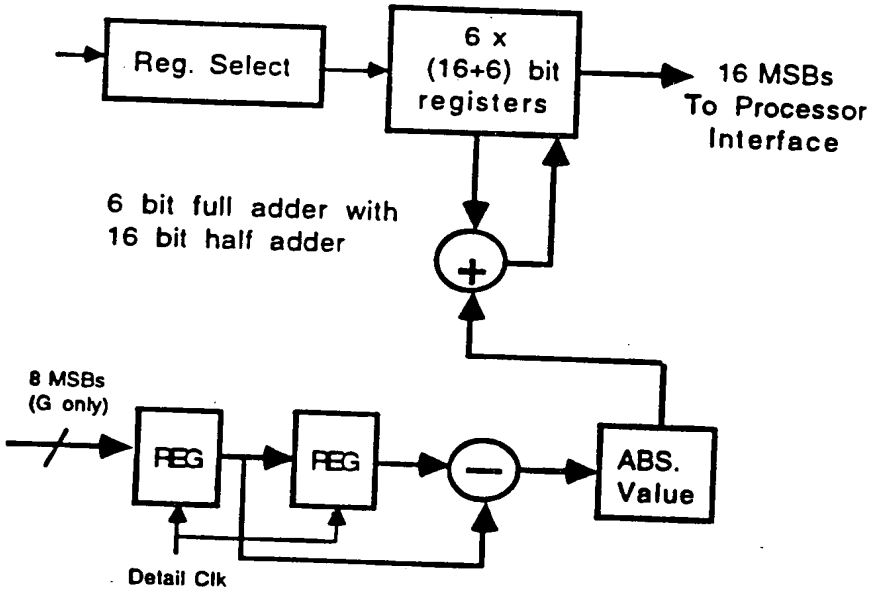
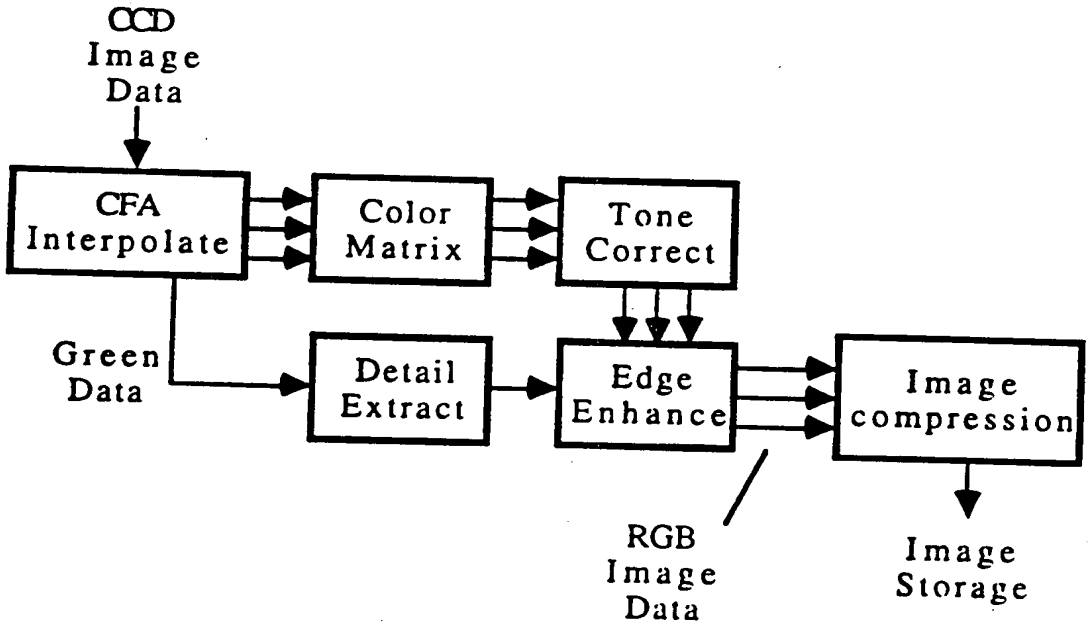


FIG. 9B

Fig. 10 Still Mode Image Processing



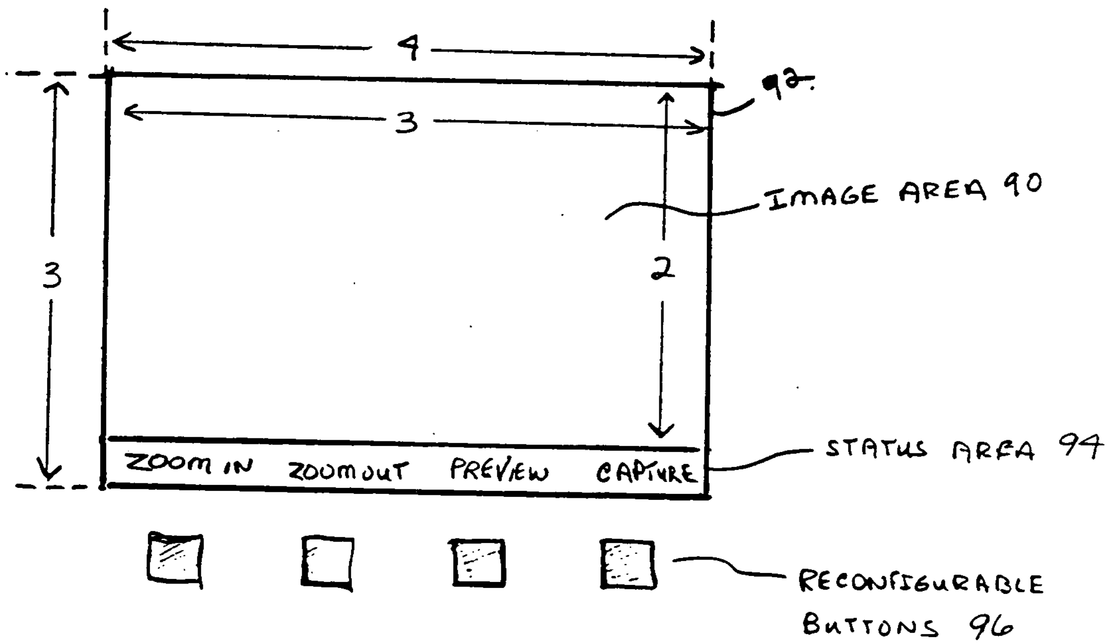

4
3
92
IMAGE AREA 90
3
2
ZOOM IN
ZOOM OUT
PREVIEW
CAPTURE
STATUS AREA 94
RECONFIGURABLE
BUTTONS 96

FIG. 11

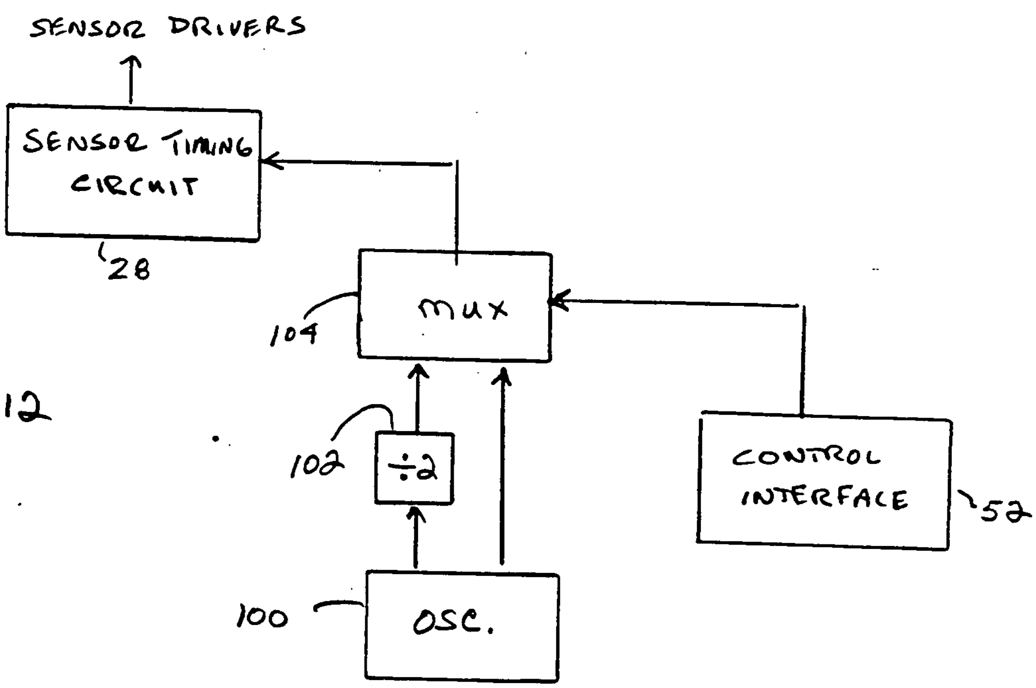

SENSOR DRIVERS
SENSOR TIMING
CIRCUIT
28
MUX
104
102
÷2
CONTROL
INTERFACE
52
100
OSC.

FIG. 12